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1. Instruction Set Architecture (ISA) selection logic within a CPU for selecting an ISA decoding mode for a program instruction from a plurality of ISA decoding modes, the program instruction retrieved from an address in an address space of the CPU, the selection logic comprising:

a plurality of boundary address registers for storing boundary addresses that partition the address space into a plurality of address ranges corresponding to the plurality of ISA decoding modes; and

ISA mode selection logic, coupled to said plurality of boundary address registers, for receiving the address, and for comparing the address to said boundary addresses to determine the ISA decoding mode for the program instruction.

2. The selection logic as recited in claim 1, wherein the CPU executes a multiple-ISA application program.

3. The selection logic as recited in claim 2, wherein said multi-ISA application program comprises program components having program instructions corresponding to said plurality of ISA decoding modes.

4. The selection logic as recited in claim 3, wherein said program instructions that correspond to a first ISA

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decoding mode are located within a first one of said plurality of address ranges.

5. The selection logic as recited in claim 1, wherein each of said plurality of boundary address registers stores a boundary address for a corresponding address range.

6. The selection logic as recited in claim 5, wherein said boundary address comprises a lower address boundary for said corresponding one of said plurality of address ranges.

7. The selection logic as recited in claim 6, wherein said ISA mode selection logic determines that a particular boundary address register corresponds to one of said plurality of address ranges within which said address is located.

8. The selection logic as recited in claim 7, wherein said ISA mode selection logic selects the ISA decoding mode corresponding to said particular boundary address register.

9. The selection logic as recited in claim 8, wherein said ISA mode selection logic provides the ISA decoding mode to instruction decoding logic to enable correct decoding of the program instruction.

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10. An Instruction Set Architecture (ISA) mode selection apparatus in a CPU, comprising:

decoding logic, for decoding a program instruction retrieved from an address within an address space of the CPU;

a boundary address register file, for storing boundary addresses that map one or more ISA modes of the CPU to corresponding address ranges within said address space; and

an ISA mode controller, coupled to said boundary address register file, and to said decoding logic, for designating to said decoding logic an ISA mode to be used to decode said program instruction according to said address.

11. The ISA mode selection apparatus as recited in claim 10, wherein said program instruction is within an application program that comprises components, each of said components having program instructions that correspond to only one of said one or more ISA modes.

12. The ISA mode selection apparatus as recited in claim 11, wherein first program components corresponding to a first ISA mode are located within a first address range.

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13. The ISA mode selection apparatus as recited in claim 10, wherein said boundary address register file comprises:

a plurality of boundary address registers, each storing one of said boundary addresses.

14. The ISA mode selection apparatus as recited in claim 13, wherein said boundary addresses comprise lower address boundaries for said corresponding address ranges.

15. The ISA mode selection apparatus as recited in claim 14, wherein said ISA mode controller comprises address evaluation logic for determining which one of said plurality of boundary address registers corresponds to said program instruction.

16. The ISA mode selection apparatus as recited in claim 15, wherein said ISA mode controller designates to said decoding logic said ISA mode based upon determining which one of said plurality of boundary address registers corresponds to the program instruction.

17. The ISA mode selection apparatus as recited in claim 10, wherein said ISA mode controller provides said ISA mode to said decoding logic to enable correct processing of said program instruction.

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18. A CPU for executing a multiple-ISA program, comprising:
ISA mode selection logic, configured to provide a first ISA mode indicator that corresponds to a first program instruction, said first program instruction being fetched from a first address in memory;
ISA mode boundary address registers, coupled to said ISA mode selection logic, configured to store boundary addresses that partition said memory into address ranges, wherein a plurality of ISA modes is mapped to said address ranges; and
an instruction decoder, coupled to said ISA mode selection logic, configured to receive said first ISA mode indicator, and configured to decode said first instruction according to said first ISA mode.

19. The CPU as recited in claim 18, wherein the multiple-ISA program comprises components that are stored within a corresponding address range.

20. The CPU as recited in claim 18, wherein said ISA mode boundary address registers contain said boundary addresses that designate said address ranges.

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21. The CPU as recited in claim 20, wherein said boundary addresses comprise lower address boundaries for said address ranges.

22. The CPU as recited in claim 21, wherein said ISA mode selection logic determines which one of said ISA mode boundary address registers corresponds to first address.

23. The CPU as recited in claim 22, wherein said ISA mode selection logic provides said first ISA mode indicator to said instruction decoder to enable correct processing of said first program instruction.

24. A computer program product for use with a computing device, the computer program product comprising:
a computer usable medium, having computer readable program code embodied in said medium, for causing a CPU to be described, said CPU for executing a multiple-ISA application program, said computer readable program code comprising:
first program code, for providing boundary address registers, configured to partition an address space of said CPU into address ranges, said address ranges corresponding to associated ISA modes; and

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second program code, for providing ISA mode selection logic, configured to receive an address from which a program instruction was retrieved, and configured to compare said address against said address ranges to determine an ISA mode for processing said program instruction.

25. The computer program product as recited in claim 24, wherein said multiple-ISA application program comprises program components corresponding to said associated ISA modes.

26. The computer program product as recited in claim 25, wherein each of said boundary address registers contains an address boundary for a corresponding address range.

27. The computer program product as recited in claim 26, wherein said address boundary comprises a lower address boundary for said corresponding address range.

28. The computer program product as recited in claim 27, wherein said ISA mode selection logic determines a particular boundary address register that corresponds to said address.

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29. The computer program product as recited in claim 28, wherein said ISA mode selection logic determines said ISA mode that corresponds to said particular boundary address register.

30. A method in a CPU for selecting an Instruction Set Architecture (ISA) mode during execution of an application program, the application program having program instructions according to a plurality of ISA modes, the method comprising:

a) partitioning an address space of the CPU into address ranges, the address ranges being designated by contents of a boundary register file;

b) mapping each of the address ranges to each of a plurality of ISA modes; and

c) selecting the ISA mode for processing of the program instruction according to said mapping.

31. The method as recited in claim 30, wherein said partitioning comprises:

i) specifying address boundaries within registers in the boundary register file.

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32. The method as recited in claim 30, wherein said mapping comprises:

i) storing individual components of the application program within an associated address range that is designated for processing of program instructions corresponding to an associated ISA mode.

33. The method as recited in claim 32, wherein said mapping further comprises:

ii) evaluating an address of a program instruction fetched during execution of the application program against the contents of the boundary register file to determine a particular address range within which the program instruction lies.

34. A computer data signal embodied in a transmission medium, comprising:

first computer-readable program code, for providing boundary address registers, said registers being configured to partition an address space into address ranges, said address ranges corresponding to associated ISA modes.

35. The computer data signal as recited in claim 34, further comprising:

second computer-readable program code, for providing ISA mode selection logic, said ISA mode selection logic being configured to receive an address associated with a program instruction, and configured to compare said address against said address ranges to determine an ISA mode for processing said program instruction.